UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/020,723	12/07/2001	John Earl Merritt	9900	9784

7590 09/16/2005

JOHN D. COWART
TERADATA LAW IP, WHQ-4W
NCR CORPORATION
1700 S. PATTERSON BLVD.
DAYTON, OH 45479-0001

EXAMINER	
FERRIS III, FRED O	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 09/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/020,723	MERRITT ET AL.	
	Examiner	Art Unit	
	Fred Ferris	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,10-17,20-27 and 30* is/are rejected.

7)☒ Claim(s) *8,9,18,19,28 and 29* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

CF

DETAILED ACTION

1. Claims 1-30 have been presented for examination based on applicant's disclosure filed 7 December 2001. The examiner has rejected claims 1-7, 10-17, 20-27, and 30. Claims 8, 9, 18, 19, 28, and 29 are objected to.

Drawings

2. Applicant's drawings submitted on 7 December 2001 have been approved by the examiner.

Preamble of the Claims

3. The preambles of independent claims 1, 11, and 21 as presented for examination, have not been given patentable weight. Appropriate weight is given to limitations recited in the body of the claim that are needed for purpose of antecedence. "A mere statement of purpose or intended use in the preamble of a claim need not be considered in finding anticipation; however, it must be considered if the language of a preamble is necessary to give meaning to the claim" Diversitech Corp. v. Century Steps, Inc., 7 USPQ2d 1315 (Fed. Cir. 1988); In re Stencel, 4 USPQ2d 1071 (Fed. Cir. 1987)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1-7, 10-17, 20-27, and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Application 2003/0037185 issued to Davis in view of U.S. Patent Application 2003/0112094 issued to Pederson et al.

Independent claims 1, 11, and 21 are drawn to:

Method, system, and computer code for executing database transactions by:
- defining interconnected nodes in terms of processor/storage resources of parallel computing system;

- mapping first virtual processors to subset of nodes to create map with virtual processor mapped to each node in first subset
- mapping second virtual processors to subset of nodes to create map with virtual processor mapped to each node in second subset
- storing first/second map as configuration
  - executing transaction using first set of virtual processors and simultaneously executing transaction using the second set of virtual processors.

Regarding independent claims 1, 11, and 21: Davis discloses defining interconnecting nodes (abstract, para: 008, 0023, Figs. 3, 5, 6) in terms of storage resources (para: 005-008, Figs. 1, 6A, 6B) in parallel processing (multiprocessor) computing system inclusive of mapping virtual resources as node sets (para: 0008). Davis further discloses that the processor resources are mapped to first and second (para: 0011, 0012, 0026, Fig. 3) node group mappings (i.e. the mapping groups are functionally equivalent to "sets" and "subsets" by including replacement nodes, para: 0029) inclusive of the system and I/O resource requirements (i.e. configuration, para: 0024).

Davis does not explicitly disclose interconnecting nodes that represent virtual processors executing transactions.

Pederson teaches defining interconnecting nodes that represent virtual processors in a parallel computing system (para: 0031) inclusive of executing transactions (para: 0036-0045) based on groups (para: 0036, 0039, 0051, i.e. sets) relating data storage (database) facilities (resources) in a distributed parallel processing system. Pederson further discloses the simultaneous execution (para: 0029) of the related transactions over the parallel system.

It would have been obvious to one having ordinary skill in the art at the time the

claimed invention was made to modify the teachings of Davis relating to defining interconnecting nodes and mapping of virtual resources in a parallel processing system, with the teachings of Pederson relating to virtual processors executing transactions , to realize the elements of the claimed invention. An obvious motivation exists since, in this case, the Davis reference teaches to the Pederson reference, and the Pederson reference teaches to the Davis reference. Specifically, both Davis and Pederson teach defining interconnected nodes in parallel processing systems and both are used in the same technological arena as noted above. Davis teaches to Pederson because Davis teaches defining interconnecting nodes that includes mapping of virtual processing resources. Pederson teaches to Davis because Pederson specifically teaches defining the interconnecting nodes of virtual processors executing transactions. (See: Pederson: para: 0036) Further, the level of skill required by an artisan to realize the claimed limitations of the present invention is clearly established by both references. (See: Davis/Pederson, Abstract) Accordingly, a skilled artisan tasked with realizing a system and method for executing database transactions by defining interconnected node and mapping sets of virtual processors, and having access to the teachings of Davis and Pederson, would have knowingly modified the teachings of Davis with the teachings of Pederson (or visa versa) to realize the claimed elements of the present invention while reducing the cost and development time.

Per dependent claims 2, 4, 12, 14, 22, and 24: These claims include additional limitations relating to exception based on failed and restored nodes and are rendered

obvious in view of the teachings of the substitute node (restored) and handicapped node (failed) disclosed by Davis (para: 0029).

Per dependent claims 3, 5, 6, 13, 15, 16, 23, 25, and 26: These claims include additional limitations relating to a third mapping, halting transactions, and use of virtual processors that are mapped to failed nodes. These limitations are therefore rendered obvious by Davis, since Davis discloses a third and forth mapping of the resources (para: 0031-0034, Figs. 5-6B) and modifying the resource map in response to failed components (para: 0031-0034, Figs. 5-6B). Pederson teaches terminating the transaction task (para: 0036-0045) and would have knowingly been incorporated by a skilled artisan using the same reasoning as previously cited above.

Per dependent claims 7, 17, and 27: As noted above, Pederson teaches executing a database transaction. Obviously a skilled artisan would have known to use a configuration table in associating the execution of transactions as a method of storing a list of records (i.e. configuration data) in a relational database. (See: "table", Microsoft Computer Dictionary, 1997)

Per dependent claims 10, 20, and 30: As also previously cited above, Pederson teaches discloses the simultaneous execution (para: 0029) of the related transactions over the parallel system and hence would have knowingly been incorporated by a skilled artisan using the reasoning cited above.

Allowable Subject Matter

5. Claims 8, 9, 18, 19, 28, and 29 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. In this case the prior art of record does not disclose the specific sequences of steps relating to executing a transaction by identifying tasks and storage resources for completing transactions, defining groups of virtual processors and transaction groups having access to storage resources, assigning tasks and groups including virtual processors having access, and completing the tasks via virtual processors assigned to the transaction group as specifically recited in dependent claims 8, 18, and 28.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

"Cellular Disco: resource management using virtual clusters on shared-memory multiprocessors", ACM Transactions on Computer Systems, Vol. 18, No. 3, ACM 2000 teaches node resource mapping of virtual processors.

U.S. Patent 6,745,240 issued to Denman et al teaches node resource mapping of virtual processors.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fred Ferris whose telephone number is 571-272-3778 and whose normal working hours are 8:30am to 5:00pm Monday to Friday. Any inquiry of a general nature relating to the status of this application should be directed to the group receptionist whose telephone number is 571-272-3700. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jean Homere can be reached at 571-272-3780. The Official Fax Number is: (703) 872-9306

Fred Ferris, Patent Examiner
Simulation and Emulation, Art Unit 2128
U.S. Patent and Trademark Office
Randolph Building, Room 5D19
401 Dulany Street
Alexandria, VA 22313
Phone: (571-272-3778)
Fred.Ferris@uspto.gov
September 14, 2005

AU 2128